What is Claimed is:

1. An analog-to-digital (A/D) converter, comprising:

a plurality of signal paths that are responsive to an analog input signal, to generate a multi-bit digital output signal therefrom; and

a circuit that is configured to generate delayed clock signals, which have delay times different from each other according to phase differences, by feeding-back and detecting a phase of signals in the signal paths, and configured to correct the signals in the signal paths by using the delayed clock signals.

2. An analog-to-digital (A/D) converter, comprising:

a clock buffer that is configured to receive and buffer an external clock signal, to thereby generate an internal clock signal;

a plurality of process routines that are configured to receive and process an analog input signal;

a plurality of comparators that are configured to receive analog signals from the plurality of process routines and to compare the received analog signals with a reference voltage, to thereby generate digital signals therefrom under control of a respective one of delayed clock signals;

a plurality of decoders that are configured to receive the digital signals from the plurality of comparators and to convert the received digital signals into a code format, to thereby generate converted digital signals; and

a synchronizing circuit that is configured to receive the internal clock signal from the clock buffer and the digital signals from the plurality of comparators and to generate the respective delayed clock signals therefrom.

3. An A/D converter according to Claim 2, wherein the synchronizing circuit comprises:

a phase detector that is configured to receive the digital signals from the plurality of comparators, and to detect a phase difference between the digital signals;

a delay controller that is configured to receive an output signal of the phase detector, and to generate a respective time delay control signal for a respective one of the process routines, corresponding to the phase difference; and

a plurality of delay chain parts that are configured to receive the internal clock signal from the clock buffer and to generate the respective delayed clock signals, under control of a respective one of the time delay control signals.

4. An A/D converter according to Claim 3, wherein the delay controller is comprised of a plurality of shift registers.

5. An A/D converter according to Claim 2, wherein the plurality of process routines are comprised of folding/interpolation and/or flash process routines.

6. An A/D converter according to Claim 3, wherein the plurality of process routines are comprised of folding/interpolation and/or flash process routines.

7. An analog-to-digital (A/D) converter, comprising:

a plurality of signal paths that are responsive to an analog input signal, to generate a multi-bit digital signal therefrom, a respective signal path including therein a comparator; and

a synchronizing circuit that is responsive to a clock signal and outputs of the comparators, to generate a respective delayed clock signal that is applied to a respective comparator.

8. An A/D converter according to Claim 7 wherein the respective signal path also includes therein a respective decoder that is responsive to the respective comparator and to the clock signal.

9. An A/D converter according to Claim 7 wherein the synchronizing circuit is configured to generate the respective delayed clock signal based on at least one phase difference between the outputs of the comparators.

10. An A/D converter according to Claim 8 wherein the synchronizing circuit is configured to generate the respective delayed clock signal based on at least one phase difference between the outputs of the comparators.

11. A synchronizing method for an analog-to-digital (A/D) converter that includes a plurality of signal paths that are responsive to an analog input signal, to generate a multi-bit digital signal therefrom, a respective signal path including therein a comparator, the synchronizing method comprising:

generating a plurality of delayed clock signals from a clock signal and outputs of the comparators; and

applying a respective one of the delayed clock signals to a respective comparator.

12. A method according to Claim 11 wherein the respective signal path also includes therein a respective decoder that is responsive to the respective comparator, the method further comprising:

applying the clock signal to the respective decoders.

13. A method according to Claim 11 wherein generating the plurality of delayed clock signals comprises generating the plurality of delayed clock signals based on at least one phase difference between the outputs of the comparators.

14. A method according to Claim 12 wherein generating the plurality of delayed clock signals comprises generating the plurality of delayed clock signals based on at least one phase difference between the outputs of the comparators.